STEM Workshop 2014

Thursday 29 /05/2014

16:00 – 16:10 Welcome: *Manuel J. Barragán*, TIMA, France, and *Gilgas Léger*, IMSE-CNM, Spain

16:10 – 17:00 Keynote: Exploiting Non-Uniformity and Correlations in Testing, *Adit Singh*, Auburn University, USA

Abstract: The testing of digital and mixed signal integrated circuits is a problem that grows exponentially with circuit size. Because complete functional testing for most circuits is totally impractical, effective test strategies must take advantage of the observed defects statistics and prioritize detection of the most likely failure modes. In this talk we show how non-uniformity and correlations in the underlying defect distributions and circuit parameters are being exploited by new statistical and adaptive test methods, with the ambitious goal of achieving "zero defect" product quality.

17:00 – 17:20 Coffee Break

17:20 – 18:20 Session 1: Reliability and model redundancy

- *Elena I. Vatajelu, M. Indaco, R. Rodriguez-Montañés, S. Di Carlo, P. Prinetto, and J. Figueras,* Spin-Torque Transfer MRAM Statistical Reliability Prediction

- *H. Ayari, F. Azais, S. Bernard, M. Comte, V. Kerzerho, S. Larguech, and M. Renovell,* Investigations on alternate analog/RF test with model redundancy

Friday 30/05/2014

9:30 – 10:30 Keynote: Statistical correlation driven testing, process diagnosis and tuning: the alternative testing paradigm and beyond, *Abhijit Chatterjee*, GeorgiaTech, USA

Abstract: Trends towards high levels of heterogeneous device integration and advanced technology scaling have escalated mixed-signal SoC test costs. The large numbers of performance specifications associated with today's mixed-signal systems makes measurement of each of these specifications for every manufactured device a very expensive proposition. Consequently, there has been renewed interest in reducing the volume of tests performed per device using a variety of methods that range from designing specialized *alternative tests* that implicitly test for all the device specifications, to use of *virtual probing* algorithms that help reduce wafer level testing effort from wafer-probe test measurement and e-test data. In this talk, a holistic cross-layer test optimization framework is proposed that leverages the benefits of the alternative test approach as well as those of orthogonal virtual probing methods. It is shown how statistical cause-effect analysis methods can be used to diagnose process parameters from test measurements on a per-chip basis allowing fine-grained detection of process shifts. It is also shown how such methods can be used to significantly reduce the cost of tuning mixed-signal/RF devices, post-manufacture, to improve device yield. Directions for future research will be discussed.

10:30 – 10:50 Coffee break

10:50 – 12:20 Session 2: Feature selection for indirect measurements

- *Álvaro Gómez-Pau, Luz Balado, and Joan Figueras,* Criteria for Indirect Measurements in M-S Testing

- *Matthieu Verdy, Alin Ratiu, Dominique Morche, Emeric De Foucauld, Suzanne Lesecq, Jean-Pascal Mallet, and Cedric Mayor,* Weight based Feature Selection Algorithm for Alternative Measurements

- *Manuel J. Barragan, and Gildas Leger,* Feature selection for Alternate Test using wrappers: application to an RF LNA case study

12:20 – 13:30 Lunch

13:30 – 14:30 Session 3: Analog fault models

- *Haralampos-G. Stratigopoulos, and Stephen Sunter,* Fast Monte Carlo-Based Estimation of Analog Parametric Test Metrics

- *Stephen Sunter,* An analysis of random sampling for analog fault simulation

14:30 – 14:40 Closing: *Manuel J. Barragán*, TIMA, France, and *Gilgas Léger*, IMSE-CNM, Spain