Program

19th IEEE European Test Symposium

May 26 - 30, 2014, Paderborn

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and everything in between

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Foreword

On behalf of the Steering, Program and Organizing Committees, we would like to welcome you to the European Test Symposium 2014 (ETS'14), the largest event in Europe entirely devoted to presenting and discussing scientific trends, emerging results, hot topics, and applications in the area of electronic circuit and system testing.

ETS'14 is the 19th edition of the symposium and is held in Paderborn, Germany. Paderborn is located in the heart of Germany between the North German lowlands and the low mountain ranges in the south. Its long history dates back to the time of Charlemagne, and today the university town of Paderborn successfully combines historical tradition with technological advances. Paderborn's special relation to information technology is demonstrated by the presence of more than 200 IT companies in the region. Moreover, the conference venue, the Heinz Nixdorf Forum, hosts the largest computer museum in the world.

ETS'14 continues its well-established format, by starting on Monday, May 26th with tutorials, followed by a three-day technical program, together with an attractive social event, and by ending on Friday, May 30th with several workshops. For the fifth time, the Test Spring School (TSS) is also organized back-to-back with ETS.

The symposium's technical program consists of two plenary keynote addresses, scientific paper presentations, three embedded tutorials, two special sessions, two vendor presentation sessions, three poster sessions, and a plenary panel. For the first time, the ETS^2-track on emerging test solutions provides a one-day informal forum for discussing upcoming problems and solutions in the test industry. ETS is a cornerstone of the "European Test Week" that also includes several test-related fringe events and the workshops on Trustworthy Manufacturing and Utilization of Secure Devices (TRUDEVICE), Statistical Test Methods (STEM), and Resource-Awareness and Adaptivity in Multi-Core Computing (RACING).

ETS'14 has received a large number of contributions from all over the world, submitted as scientific papers, special session proposals, embedded tutorials, and vendor presentations. All submissions underwent a rigorous review process. Five reviewers have examined every scientific paper on average. All submitted papers were discussed and evaluated at the full-day

PC meeting on January 31st, 2014, in Poznan, Poland. As a result, 28 scientific papers and 27 posters were selected for inclusion into the ETS'14 Formal Proceedings, an electronic version of which is distributed to all attendees on a USB stick. The authors of embedded tutorial and special session papers were also given the opportunity to publish an overview paper in the formal proceedings. Vendor papers and other informal contributions were added to the material on the USB stick on request. Authors of the best paper presented at ETS'14 will receive an award during the next year's edition of ETS.

A successful ETS'14 would not be possible without individual contributions of many volunteers. We would like to thank all of them for their efforts. We are confident that you will find ETS'14 a productive and exciting experience with lots of superb networking opportunities for researchers, developers and vendors.

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intel

Organizers

University of Paderborn, Germany
Poznan University of Technology, Poland

Dates / Symposium Venue

May 26-30, 2014
Heinz Nixdorf MuseumsForum
Fürstenallee 7
33102 Paderborn, Germany
Phone +49 (0)5251 306 600
Web http://www.hnf.de

Registration / Information Hours

Monday, May 26	13:00-18:30	
Tuesday, May 27	08:00-12:30	14:00-18:00
Wednesday, May 28	08:00-12:30	14:00-15:00
Thursday, May 29	08:00-12:30	14:00-18:00

Board

The Welcome Reception on Monday takes place in the Town Hall of Paderborn. Coffee breaks will be given in the Foyer, and lunches will be served in the Exhibition Area. On Tuesday evening a Westphalian Buffet will be served in the Bistro Hotspot.

Public Transportation

The HNF conference center is in walking distance from the Welcome Hotel (15 minutes). From the city center the conference venue can be can be reached on foot in 30 minutes or with bus No. 11. The most convenient way to get around inside the city is by walking. Nevertheless a public transportation map can be found at http://www.padersprinter.de/.

Map of the Venue

14:00-18:30 **Tutorial A** (Seminar Room 1/2)

Mixed-signal/RF design-for-test: principles and advanced techniques Salvador Mir (TIMA, FR)

14:00-18:30 **Tutorial B** (Seminar Room 3)

Production test practices - How they vary and why?
Jochen Rivoir (Advantest Europe GmbH, DE)

19:00-21:00 **Welcome Reception** (Town Hall)

Welcome Address Heinz Paus (Mayor of Paderborn)

Sponsored by the City of Paderborn

8:45-10:00 Plenary Session (Auditorium)

8:45-9:15 Opening

Welcome Address and Symposium Information Sybille Hellebrand (Paderborn U., DE – ETS'14 General Chair)

Welcome Address Nikolaus Risch (Paderborn U., DE – President of Paderborn U.)

Program Introduction Jerzy Tyszer (Poznan U. of Technology, PL – ETS'14 Program Chair)

ETS'13 Best Paper Award Zebo Peng (Linköping U., SE – ETS'13 Program Chair)

9:15-10:00 Keynote

Major Eras of Design for Test Walden C. Rhines (CEO of Mentor Graphics Corp., US)

From writing functional tests to managing design groups to managing major businesses, Dr. Rhines has been personally involved in the evolution of Design for Test. From this perspective, he will describe the driving forces and technologies that changed the way we design products to make them testable, and what will drive change in the future.

10:00-11:00 Posters & Coffee (Foyer)

Poster Session 1

Chair: Ozgur Sinanoglu (New York U. Abu Dhabi, AE)

P1.1 A Distance-Based Test Cube Merging Procedure for Compatible and Incompatible Test Cubes I. Pomeranz (Purdue U., US)

P1.2 Logic Simulation and Fault Collapsing with Shared Structurally Synthesized BDDs D. Mironov, R. Ubar, J. Raik (Tallinn U. of Technology, EE)

P1.3 Analysis of Cell-Aware Test Pattern Effectiveness – A Case Study Using a 32-bit Automotive Microcontroller A. Prabhu (Freescale, Darmstadt U., DE), V. Vorisek, H. Lang (Freescale, DE), T. Schumann (Darmstadt U.,

DE)

P1.5 A Generic and High-Level Model of Large Unreliable NOCs for Fault Tolerance and Performance Analysis F. Chaix, N.-E. Zergainoh, M. Nicolaidis (TIMA, FR)

P1.6 Property-Checking Based LBIST for Improved Diagnosability S. Prabhu, V.V. Acharya, S. Bagri, M.S. Hsiao (Virginia Tech, US)

P1.7 A Collision Resistant Deterministic Random Bit Generator with Fault Attack Detection Possibilities E. Böhl, M. Lewis, K. Damm (Bosch, DE)

P1.8 iBoX – Jitter Based Power Supply Noise Sensor M. Valka, A. Bosio, L. Dilillo, A. Todri, A. Virazel, P. Girard (LIRMM, FR), P. Debaud, S. Guilhot (ST-Microelectronics, FR)

P1.9 A Novel Adaptive Fault Tolerant Flip-Flop Architecture based on TMR L. Cassano (Pisa U., Poli. di Milano, IT), A. Bosio, G. Di Natale (LIRMM, FR)

11:00-12:30 Session 2A (Seminar Room 1/2)

Soft Errors in Processors

Chairs: Zebo Peng (Linköping University, SE), Jaan Raik (Tallinn University of Technology, EE)

2A.1 Two Soft-Error Mitigation Techniques for Functional units of DSP Processors A. Rohani, H. G. Kerkhoff (Twente U., NL)

2A.2 Reducing Embedded Software Radiation-Induced Failures Through Cache Memories T. Santini, P. Rech, G. Nazar, L. Carro, F. Rech Wagner (Federal U. Rio Grande do Sul, BR)

2A.3 Detection Conditions for Errors in Self-adaptive Better-than-worst-case Designs I. Polian, J. Jiang (Passau U., DE), A. Singh (Auburn U., US)

ETS^2 is a new initiative to be held for the first time during ETS2014. The ETS^2 sessions are characterized by an industrial focus and by flexibility and informality. Consequently, the agenda as listed below is subject to change. During the actual day there may be a switch from one topic to another, and back, depending on the discussions. Also the order of the listed presentations may change, even on the fly. The main goal is to have a lively discussion on the topics, on the presentations. The ETS^2 should act as a podium to discuss both problems as well as potential solutions, in order to motivate all involved, industry and academia, to move forward in the broad area of Test.

11:00-12:30 Session 2B (Seminar Room 3)

ETS^2

Chairs: Rene Segers (ReSeCo, NL), Matteo Sonza-Reorda (Poli. di Torino, IT), Stefan Eichenberger (NXP, DE)

2B.1 Automotive (Test) Experiences and Requirements in NXP R. van Rijsinge (NXP, NL)

2B.2 The Importance of Reliable Data A. van de Geijn (Salland Engineering, NL)

2B.3 Testing for Yield Learning, THE added value of Test T. Hermann (GLOBALFOUNDRIES, DE)

2B.4 DPCV - Direct Probe Product Characterization Vehicle Applications, Methodology and Benefits B. Murugan, M. Lunenborg (PDF Solutions, US)

12:30-14:00 Lunch (Exhibition Area)

14:00-15:30 Session 3A (Seminar Room 1/2)

Diagnosis and Debug

Chairs: Elham Moghaddam (Mentor Graphics, US), Stephan Eggersglüss (Bremen U., DE)

3A.1 Systematic Generation of Diagnostic Software-Based Self-Test Routines for Processor Components M. Schölzel, T. Koal, H. T. Vierhaus (BTU Cottbus, DE)

3A.2 Diagnosis of Multiple Faults with Highly Compacted Test Responses A. Cook, H.-J. Wunderlich (Stuttgart U., DE)

3A.3 Improving Polynomial Datapath Debugging with HEDs S. Sadeghi-Kohan, P. Behnam, B. Alizadeh (Tehran U., IR), M. Fujita (Tokyo U., JP), Z. Navabi (Tehran U., IR)

14:00-15:30 Session 3B (Seminar Room 3)

ETS^2 Continued

Chairs: Rene Segers (ReSeCo, NL), Matteo Sonza-Reorda (Politecnico di Torino, IT), Stefan Eichenberger (NXP, DE)

3B.1 Telecom (Test) Requirements and Experiences in Huawei X. Gu (Huawei, US)

3B.2 Analog DfT & Test, Experiences and Outlook in AMD J. Rearick (AMD, US)

3B.3 Analog DfT & Test, Experiences and Outlook, PoV from an EDA company S. Sunter (Mentor Graphics, CA)

3B.4 Analog DfT & Test: Implementing Analog Iddq P. Sarson (AMS, AT)

15:30-16:15 Posters & Coffee (Foyer)

Poster Session 2

Chair: Helmut Lang (Freescale Semiconductor, DE)

P2.1 Towards a General Purpose Mixed-Signal Instrumentation Layer in the Die Stack of a 3D-IC S. Lin, G. W. Roberts (McGill U., CA)

P2.2 Automatic Correction of Certain Design Errors Using Mutation Technique P. Behnam, B. Alizadeh, Z. Navabi (Tehran U., IR)

P2.3 Power Efficient Scan Testing by Exploiting Existing Error Tolerance Circuitry in a Design A. Anastasiou, Y. Tsiatouhas (Ioannina U., GR)

P2.4 GPU-Based Timing-Aware Test Generation for Small Delay Defects K.-Y. Liao, P.-J. Chen, A.-F. Lin, J. C.-M. Li (National Taiwan U., TW), M. S. Hsiao (Virginia Tech, US), L.-T.

Wang (SynTest Technologies, US)

P2.5 Accumulator-based Test-per-clock Scheme for Low-power On-chip Application of Test Patterns I. Voyiatzis (Technological Educational Inst. of Athens, GR)

P2.6 Quantitative Evaluation of Register Vulnerabilities in RTL Control Paths L. Chen, M. Ebrahimi, M. B. Tahoori (Karlsruhe Inst. of Technology, DE)

P2.7 Design of Low Cost Fault Tolerant Analog Circuits Using Real-Time Learned Error Compensation S. Banerjee (Georgia Inst. of Technology, US), A. Gómez-Pau (Poli. de Catalunya, ES), A. Chatterjee (Georgia Inst. of Technology, US)

P2.8 Homogeneous Many-core Processor System Test Distribution and Execution Mechanism A. Kamran, Z. Navabi (Tehran U., IR)

16:15-17:45 Session 4A (Seminar Room 1/2)

Security

Chairs: Mohamed Azimane (NXP, NL), Ioana Elena Vatajelu (Poli. di Torino, IT)

4A.1 Test-Mode-Only Scan Attack Using the Boundary Scan Chain S.S. Ali, O. Sinanoglu (New York U. Abud Dhabi, AE), R. Karri (New York U., US)

4A.2 A True Random Number Generator with On-Line Testability E. Böhl, M. Lewis (Bosch, DE), S. Galkin (Hochschule Pforzheim, DE)

4A.3 A New Efficiency Criterion for Security Oriented Error Correcting Codes Y. Neumeier, O. Keren (Bar-Ilan U., IL)

16:15-17:45 Session 4B (Seminar Room 3)

ETS^2 Continued

Chairs: Rene Segers (ReSeCo, NL), Matteo Sonza-Reorda (Poli. di Torino, IT), Stefan Eichenberger (NXP, DE)

4B.1 Analog DfT/Test Experiences in Freescale H. Lang (Freescale, DE)

4B.2 NFF, No Failures Found, How to Learn from them A. Jutman (Testonica, EE)

4B.3 A New Way to Catch Defects that Escape Production Test but Show Up in SLT or as RMA H. Chen (Mediatek, US)

4B.4 Operational Test Business in Europe F. Mauron (Aptasic, CH)

17:45-18:00 **Break**

18:00-19:30 **Session 5** (Exhibition Area)

Wine and Cheese Panel: Ask the Experts!

Organizer: Jeff Rearick (AMD, US)

19:30-21:30 **Westphalian Buffet** (Bistro Hotspot)

8:45-9:30 Session 6 (Auditorium)

Keynote

Factoring Variability in the Design/Technology Co-Optimisation (DTCO) in advanced CMOS Asen Asenov (Glasgow U., UK)

This presentation describes the fully automated GSS tool flow, which bridges the gap between Technology Computer Aided Design (TCAD) at the transistor level, and circuit simulations and verification. The purpose of the tool flow is twofold: (i) to allow rapid simulation-based Design Technology Co-Optimisation (DTCO) and (ii) to allow generation of accurate compact models for Preliminary Design Kit (PDK) development at the early stages of new technology development. The aim is to capture accurately process, statistical and time dependent variability in the DTCO and early PDKs. The operation of the automated tool flow is exemplified in the comprehensive PDK compact model development for a 14 nm SOI FinFET process, and the corresponding transistor / SRAM cell co-optimisation.

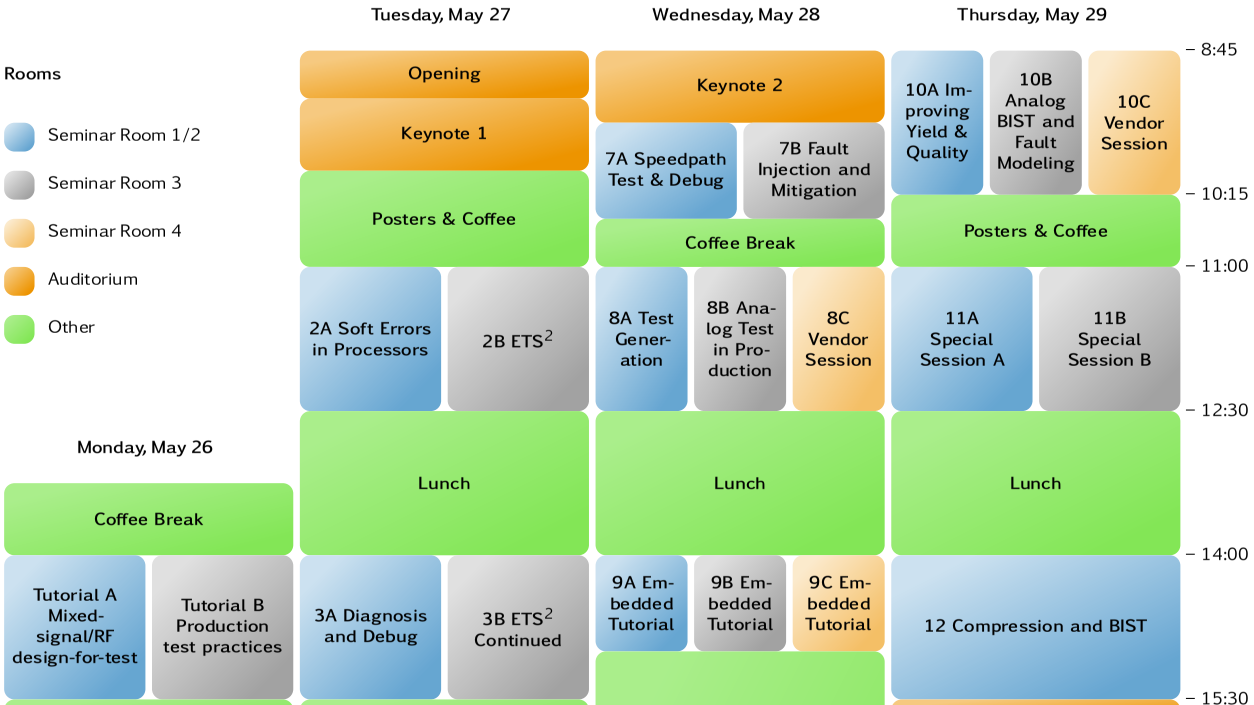
9:30-10:30 Session 7A (Seminar Room 1/2)

Speedpath Test and Debug

Chairs: Friedrich Hapke (Mentor Graphics, DE), Matteo Sonza-Reorda (Poli. di Torino, IT)

7A.1 Shadow-scan design with low latency overhead and in-situ slack-time monitoring S. Sarrazin, S. Evain (CEA, LIST, FR), I. Miro-Panades, A. Valentian (CEA, LETI, FR), S. Pajaniradja (CEA, LIST, FR), L. A. de Barros Naviner (Telecom ParisTech, FR), V. Gherman (CEA, LIST, FR)

7A.2 SAT-Based Speedpath Debugging Using Waveforms M. Dehbashi (DLR, Bremen U., DE), G. Fey (DFKI, Bremen U., DE)


Rooms
Seminar Room 1/2
Seminar Room 3
Seminar Room 4
Auditorium
Other
Monday, May 26
Coffee Break
Tutorial A Mixed-signal/RF design-for-test
Tutorial B Production test practices
Lunch
Coffee Break
Tuesday, May 27
Opening
Keynote 1
Posters & Coffee
2A Soft Errors in Processors
2B ETS2
Lunch
3A Diagnosis and Debug
3B ETS2 Continued
Wednesday, May 28
Keynote 2
7A Speedpath Test & Debug
7B Fault Injection and Mitigation
Coffee Break
8A Test Generation
8B Analog Test in Production
8C Vendor Session
Lunch
9A Embedded Tutorial
9B Embedded Tutorial
9C Embedded Tutorial
Thursday, May 29
10A Improving Yield & Quality
10B Analog BIST and Fault Modeling
10C Vendor Session
Posters & Coffee
11A Special Session A
11B Special Session B
Lunch
12 Compression and BIST
8:45
10:15
11:00
12:30
14:00
15:30


Coffee Break
Posters & Coffee
Tutorial A
Tutorial B
4A Security
4B ETS^2 Continued
Wine and Cheese Panel: Ask the Experts!
Welcome Reception
Westphalian Buffet
Social Event
Closing Ceremony
ETS Fringe Workshops
15:30
16:00
18:00
19:00
19:30
21:00

9:30-10:30 Session 7B (Seminar Room 3)

Fault Injection and Mitigation

Chairs: Krish Chakrabarty (Duke U., US), Ilia Polian (Passau U., DE)

7B.1 Smart-Hopping: Highly Efficient ISA-Level Fault Injection on Real Hardware H. Schirmeier, L. Rademacher, O. Spinczyk (TU Dortmund, DE)

7B.2 Analysis and Mitigation of Single Event Effects on Flash-based FPGAs L. Sterpone, B. Du (Poli. di Torino, IT)

10:30-11:00 Coffee Break (Foyer)

11:00-12:30 Session 8A (Seminar Room 1/2)

Test Generation

Chairs: Grzegorz Mrugalski (Mentor Graphics, PL), Bruno Rouzeyre (LIRMM, FR)

8A.1 Incremental Computation of Delay Fault Detection Probability for Variation-Aware Test Generation M. Wagner, H.-J. Wunderlich (Stuttgart U., DE)

8A.2 Variation-Aware Deterministic ATPG M. Sauer (Freiburg U., DE), I. Polian (Passau U., DE), M. E. Imhof, A. Mumtaz, E. Schneider (Stuttgart U., DE), A. Czutro (Freiburg U., DE), H.-J. Wunderlich (Stuttgart U., DE), B. Becker (Freiburg U., DE)

8A.3 Optimization-based Multiple Target Test Generation for Highly Compacted Test Sets S. Eggersglüss, K. Schmitz (DFKI, Bremen U., DE), R. Krenz-Baath (Hochschule Hamm-Lippstadt, DE), R. Drechsler (DFKI, Bremen U., DE)

11:00-12:30 Session 8B (Seminar Room 3)

Analog Test in Production

Chairs: Florence Azais (LIRMM, FR), Alexios Spyronasios (Dialog Semiconductor, DE)

8B.1 Site Dependencies in a Multisite Testing Environment T. Lehner (ELMOS Semiconductor, DE), A. Kuhr (NOFFZ Computer Technik, DE), M. Wahl, R. Brück (Siegen U., DE)

8B.2 M-S Specification Binning Based on Digitally Coded Indirect Measurements A. Gómez-Pau, L. Balado, J. Figueras (U. Poli. de Catalunya, ES)

8B.3 Avoiding Burnt Probe Tips: Practical Solutions for Testing Internally Regulated Power Supplies R. Swanson, A. Wong, S. Ethirajan, A. Majumdar (Xilinx, US)

11:00-12:30 Session 8C (Seminar Room 4)

Vendor Session

Chairs: Said Hamdioui (Delft U.), Giorgio Di Natale (LIRMM, FR)

8C.1 Improving Test Quality while Reducing DFT Costs Through a Hybrid ATPG + Logic BIST Solution M. Keim (Mentor Graphics, US)

8C.2 New Solutions for Reducing the Time, Effort and Cost of Quality SoC Testing R. Kapur (Synopsys, US)

8C.3 3. ProChek: The shortcut to device and process qualification, characterization, comparison and reliability assessment H. Manhaeve (Ridgetop Europe nv, BE)

12:30-14:00 Lunch (Exhibition Area)

14:00-15:00 Session 9A (Seminar Room 1/2)

Embedded Tutorial

Chair: Bernd Becker (Freiburg U., DE)

9A.1 Error Detection and Recovery in Better-than-Worst-Case Timing Designs A. D. Singh (Auburn U., US)

14:00-15:00 Session 9B (Seminar Room 3)

Embedded Tutorial

Chair: Görschwin Fey (DFKI, Bremen U., DE)

9B.1 Fault Injection and Fault Tolerance Methodologies for Assessing Device Robustness and Mitigating against Ionizing Radiation D. Alexandrescu (IROC Technologies, FR), L. Sterpone (Poli. di Torino, IT), C. Lopez-Ongil (Carlos III U. of Madrid, ES)

14:00-15:00 Session 9C (Seminar Room 4)

Embedded Tutorial

Chair: Marie-Lise Flottes (LIRMM, FR)

9C.1 On the Impact of Process Variability and Aging on the Reliability of Emerging Memories M. Indaco, E. I. Vatajelu, P. Prinetto (Poli. di Torino, IT)

15:00-23:00 Social Event

8:45-10:15 Session 10A (Seminar Room 1/2)

Improving Yield and Quality

Chairs: Sudhakar Reddy (Iowa U., US), Liviu Miclea (Tech. U. of Cluj-Napoca, RO)

10A.1 Cell-aware Experiences in a High-Quality Automotive Test Suite F. Hapke (Mentor Graphics, DE), R. Arnold, M. Beck, M. Baby, S. Straehle, J.F. Goncalves, A. Panait, R. Behr, G. Maugard, A. Prashanthi (Infineon Technologies, DE), J. Schloeffel, W. Redemund, A. Glowatz, A. Fast (Mentor Graphics, DE), J. Rajski (Mentor Graphics, US)

10A.2 Quantified Contribution of Design for Manufacturing to Yield at 28nm T. Hermann (GLOBALFOUNDRIES, DE), S. Malik, S. Madhavan (GLOBALFOUNDRIES, US)

10A.3 Post-Bond Test of Through-Silicon Vias with Open Defects R. Rodríguez-Montañés, D. Arumí, J. Figueras (U. Poli. de Catalunya, ES)

8:45-10:15 Session 10B (Seminar Room 3)

Analog BIST and Fault Modeling

Chairs: Cedric Mayor (Presto Engineering Europe, FR), Wolfgang Vermeiren (Fraunhofer Institute for Integrated Circuits IIS, DE)

10B.1 Optimization of Analog Fault Coverage by Exploiting Defect-Specific Masking A. Coyette, G. Gielen (KULeuven, BE), R. Vanhooren, W. Dobbelaere (ON Semiconductor, BE)

10B.2 INL Systematic Reduced-Test Technique for Pipeline ADCs E. Peralías, A. Ginés, A. Rueda (Sevilla U., ES)

10B.3 Built-In Self-Calibration of CMOS-Compatible Thermopile Sensor with On-Chip Electrical Stimulus J. Li, Z. Huang, W. Wang (Chinese Academy of Sciences Beijing, CN)

8:45-10:15 Session 10C (Seminar Room 4)

Vendor Session

Chair: Hans Kerkhoff (Twente U., NL), Xiaoqing Wen (Kyushu U., JP)

10C.1 TSV BIST: An Innovative Method for 2.5D / 3D IC Interconnection Integrity Monitoring Hans Manhaeve (Ridgetop Europe nv, BE)

10C.2 Bit Error Rate Testing (BERT) using FPGA Assisted Test J. Heiber (GÖPEL electronic, DE)

10C.3 ELESIS towards Sophisticated Test Methods M. Azimane (NXP, NL)

10:15-11:00 Posters & Coffee (Foyer)

Poster Session 3

Chair: Artur Pogiel (Mentor Graphics, PL)

P3.1 Triple Error Detection for Imai-Kamiyanagi Codes Based on Subsyndrome Computations C. Badack, M. Gössel (Potsdam U., DE)

P3.2 On-the-Fly Timing-Aware Built-In Self-Repair for High-Speed Interposer Wires in 2.5-D ICs S.-Y. Huang, Z.-F. Zeng (National Tsing Hua U., TW), K.-H. Tsai, W.-T. Cheng (Mentor Graphics, US)

P3.3 Verification of the Decimal Floating-Point Square Root Operation A. S. Ahmed (Bremen U., DE), H. Fahmy (Cairo U., EG), U. Kühne (Bremen U., DE)

P3.4 Model Based Generation of High Coverage Test Suites for Embedded Systems O. Ferrante, A. Ferrari (ALES, IT), M. Marazza (Rome U., IT)

P3.5 Interleaved Scrambling Technique: A Novel Low-Power Security Layer for Cache Memories M. Neagu, L. Miclea (Technical U. of Cluj-Napoca, RO), S. Manich (Poli. de Catalunya, ES)

P3.6 Aging and Voltage Scaling Impacts under Neutron-induced Soft Error Rate in SRAM-based FPGAs F. L. Kastenschmidt, J. Tonfat, T. Both, P. Rech, G. Wirth, R. Reis (PGMICRO, PPGC, UFRGS, BR), F. Bruguier, P. Benoit, L. Torres (LIRMM, FR), C. Frost (ISIS, STFC, UK)

P3.7 Concurrent Online BIST for Sequential Circuits Exploiting Input Reduction and Output Space Compaction I. Voyiatzis (Technological Educational Inst. of Athens, GR)

P3.8 An Off-line MDSI Interconnect BIST Incorporated in BS 1149.1 M. Mohammadi, S. Sadeghi-Kohan, N. Masoumi, Z. Navabi (Tehran U., IR)

11:00-12:30 Session 11A (Seminar Room 1/2)

Special Session: Reconfigurable High Performance Architectures: How much are they ready for safety-critical applications?

Organizer and Chair: Luca Sterpone (Poli. di Torino, IT)

F 11A.1 An Open Platform for Parameterization and Dynamic Reconfiguration Support in VLIW Processors (Long Presentation) Stephan Wong, J. Hoozemans (TU Delft, NL)

11A.2 Software-based Diagnosis and Reconfiguration in VLIW Processors for Handling Permanent Faults (Short Presentation) M. Schölzel (BTU Cottbus, DE)

11A.3 Dependable FPGA-based Reconfiguration for Satellite On-Board Processing (Long Presentation) R. Glein, F. Rittner, C. Stender (ISS Fraunhofer, DE)

11A.4 Dynamically Reconfigurable Hardware for Satellite Payload Processing (Short Presentation) M. Porrmann (Bielefeld U., DE)

11:00-12:30 Session 11B (Seminar Room 3)

Special Session: Automotive Electronics

Organizer: Piet Engelke (Infineon, DE)

Chairs: Matthias Beck (Infineon, DE), Hans-Joachim Wunderlich (Stuttgart U., DE)

11B.1 Infineon's Vision on Structural Testing S. Vock (Infineon, DE)

11B.2 Automotive MEMS Sensors @ Bosch M. Lewis (Bosch, DE)

12:30-14:00 Lunch (Exhibition Area)

14:00-15:30 Session 12 (Seminar Room 1/2)

Compression and BIST

Chairs: Matthias Beck (Infineon, DE), Paolo Prinetto (Poli. di Torino, IT)

12.1 Secure and Efficient LBIST for Feedback Shift Register-Based Cryptographic Systems E. Dubrova (Royal Inst. of Technology, SE), M. Näslund, G. Selander (Ericsson Research, SE)

12.2 Using Dynamic Shift to Reduce Test Data Volume in High-Compression Designs X. Lin, M. Kassab, J. Rajski (Mentor Graphics, US)

12.3 Output-Bit Selection with X-Avoidance using Multiple Counters for Test-Response Compaction W.-C. Lien, K.-J. Lee (National Cheng Kung U.,TW), K. Chakrabarty (Duke U., US), T.-Y. Hsieh (National Yat-sen U., TW)

15:30-15:45 Closing Ceremony (Seminar Room 1/2)

ETS Fringe Workshops will be held in the Seminar Rooms from Thursday, May 29, at 16:00 up to Friday afternoon. Detailed information of the workshops is available at `http://www.ets14.de/pages/workshops/general-information.php`.

STEM Workshop: Statistical TEst Methods Workshop (Seminar Room 1/2)

General Chair: Manuel Barragan (TIMA, FR)

Program Chair: Gildas Leger (Institute of Microelectronics of Seville, SE)

Statistical test methods represent a promising step towards the reduction of the ever-increasing test costs for complex integrated systems. As opposed to traditional tests, based on extensive direct measurements, statistical test methods rely on building statistical models to infer the desired test information from simpler observables. Moreover, harvested statistical test data can be used to improve diagnosis and enable silicon-debug capabilities. The objective of this workshop is to provide an environment where researchers from academia and industry can discuss their latest findings, approaches, and ongoing work on all aspects of statistical test methods, from purely mathematical advancements to actual production test experiences.

RACING 2014: 1st Workshop on Resource-Awareness and Adaptivity in Multi-Core Computing (Seminar Room 3)

General Chair: Jürgen Teich (Erlangen-Nuremberg U., DE)

Program Chair: Frank Hannig (Erlangen-Nuremberg U., DE)

The steady advances in semiconductor technology allow for increasingly complex SoCs, including multiple (heterogeneous) microprocessors, dedicated accelerators, large on-chip memories, sophisticated interconnection networks, and peripherals. However, design, verification, and test as well as parallel programming of such complex multi-core architectures are very challenging since they may have to deal with highly dynamic

workloads in different application scenarios and environments. One recent research trend in multi-core computing is to design control loops across all platform layers – from application and run-time software down to the status of the underlying hardware. Concepts such as resource-aware programming and adaptive computing are promising candidates for optimizing multi-core systems at run-time with respect to several objectives (utilization, performance, temperature, energy, reliability, dependability, etc.) This workshop aims at bringing together researchers and experts from both academia and industry together to discuss and exchange research advances from different disciplines in design and test of multi-core architectures as well as programming and run-time management. A distinctive feature of the workshop is its cross section through the entire software/hardware stack, ranging from programming down to multi-core hardware.

TRUDEVICE Workshop on Test and Fault Tolerance for Secure Devices

(Seminar Room 4)

General Co-Chairs: Giorgio Di Natale (LIRMM, FR), Ilia Polian (Passau U., DE)

Program Chair: Marie-Lise Flottes (LIRMM, FR)

Hardware security is becoming increasingly important for many embedded systems applications ranging from small RFID tag to satellites orbiting the earth. The vulnerability of hardware devices that implement cryptography functions has become the Achille's heel in the last decade. In the framework of the COST Action IC1204 - TRUDEVICE (Trustworthy Manufacturing and Utilization of Secure Devices) this Workshop will provide an open forum for presentations in the above-mentioned fields.

FP7 STREP Project BASTION "Board and SoC Test Instrumentation for Ageing and No Failure Found"

Chair: Artur Jutman
Monday, May 26, from 12:00 to 17:00
Seminar Room 4

ETS Steering Committee Meeting

Chair: Hans-Joachim Wunderlich
Monday, May 26, from 15:00 to 18:00
Seminar Room 5

TTTC PhD Contest

Chair: Jaan Raik
Wednesday, May 28, from 11:00 to 12:00
Seminar Room 5

ETTTC Meeting

Chair: Giorgio Di Natale
Wednesday, May 28, from 12:30 to 14:00
Seminar Room 5

ETS15 Executive Committee Meeting

Chairs: Liviu Miclea, Paolo Prinetto
Thursday, May 29, from 12:30 to 14:00
Seminar Room 5

ETS14 Executive Committee Meeting

Chairs: Sybille Hellebrand, Jerzy Tyszer
Thursday, May 29, from 16:00 to 18:00
Seminar Room 5

Welcome Reception

The Welcome Reception will take place on Monday, May 26, from 19:00 to 21:00 in the Town Hall, which is located in the city center. The Mayer of Paderborn will welcome ETS participants with drinks and small snacks.

Wine and Cheese Panel

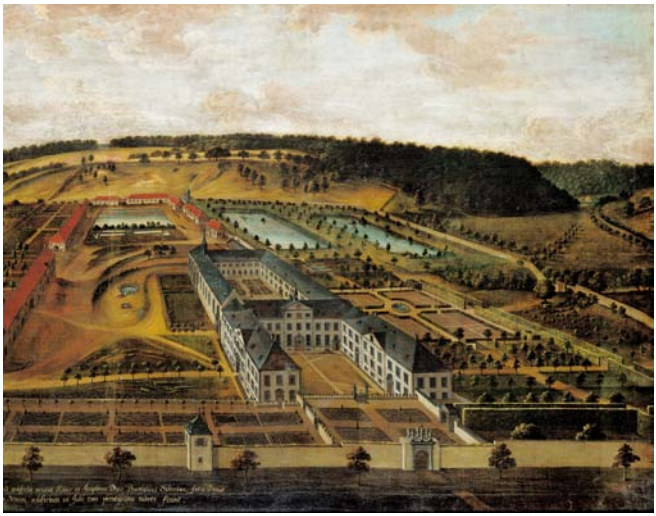
On Tuesday, May 27, the ETS panel „Ask the Experts!“ will take place from 18.00 to 19.30. Wine and cheese will be served to stimulate active participation of all attendees in this event.

Westphalian Buffet

A typical Westphalian Buffet will be served on Tuesday, May 27, from 19.30 to 21.30 in the Bistro Hotspot.

Social Event

The Social Event on Wednesday, May 28, will take place in the Monastery of Dalheim. Buses will depart from the conference venue at 15:15. The Monastery has a rich history and is now a museum of monastic culture that is unique in Germany. The visit will start with some refreshments and a brief introduction to the venue. Then there will be time to explore the exhibits, the historical buildings or enjoy the beautiful gardens. Participants can also choose between three tutorials related to monastic culture: brewing beer, distilling fruit spirit, soccer and religion.



The evening at Dalheim will start with a concert in the church at 19:00. After that aperitif and dinner will be served in the „Klosterwirtshaus“. Buses will return to Paderborn from 22:30.


Welcome Hotel
Fürstenweg
ETS
HNF
Rolandsbad
Schützenplatz
Maltaweg
Maspern-
platz
Bus No. 11
Schloß Neuhaus
B 64
A 33/A 2
Neuhäuser Straße
Paderwall
Spitalmauer
MultiCult
P3
„Neuhäuser Tor"
WC
Kisau
Am Damm
A. d. Wasserkunst
Westermauer
Königs-straße
Friedrichstraße
P10
Bachstraße
Am Abdinghof
Marienstraße
Königs-
platz
Im Dusternn
P10
P1
WC
Alte Torgasse
Wall
Bolton
Westermauer
P11
Westernstraße
Rosenstraße
Franziskaner-
kirche
Post
Franziskanermauer
Herz-Jesu-
Kirche
Florianstraße
Rathenaustraße
ca. 600 m
P2
Bahnhofstraße
Le-Mans-Wall
P12
P7
Kultur-
werkstatt
B 1/A 33/A 44
DB
Hauptbahnhof
Radstation im Hbf.
P13
Borchener Straße
B 480/
A 33 /A 44
Leostraße
Karlstraße
Killanstraße


Sportzentrum
Maspernplatz,
Schwimmoper
P 5
Rolandsweg
Am
Bischofsteich
Heierswall
Detmolder Straße
B 1
P 4
WC
Hathumarstraße
P
WoMo
P 4
Jugend-
herberge
Heiersmauer
P
Bus
Heiersmauer
WC
PaderHalle
Ükern
Heiersstraße
Mühlenstraße
Uhlenstraße
Gierswall
Städtische
Musikschule
Krämerstraße
Kapuziner-
kirche
Am Stadelhof
Giersmauer
Mühlenstraße
Auf den Dielen
Adam-u.
Eva-Haus
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Driburger Straße
B 64
Michaelstraße
Stadtbibliothek
Heiersstraße
Giersstraße
Museu m
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Erzb.
Generalvikariat
Busdorfkirche
Busdorfwall
Busdorfmauer
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Diözesanmuseum
Städtische
Galerie
Markt
Gaukirche
Am Abdinghof
Stadtver-
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Tourist Information
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Theater
Paderborn
Museum f.
sakrale Kunst
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Kasseler Straße
Marien-
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Rathaus-
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Rathauspassage
Schulmuseum
Kamp
Libori-
Galerie
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Jesuitenkirche
Kasseler Mauer
Kasseler Tor
DB
B 68
Universität
Jesuitenmauer
Warburger Straße
Leostraße
TSS
Liboriberg
Liborikapelle
P 7
P 7
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Leostraße
Husener Straße
Mallinckrodtstraße
Kilianstraße
Leostraße
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